# Digital Design Using Digilent Fpga Boards Vhdl/ Active - HDL Edition

*Richard E. Haskell*

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This book uses over 75 examples to show you how to get started designing digital circuits in VHDL, simulate them, and quickly and easily download them to your BasysTM, Nexys2TM, or Nexys3TM board. Get up and running quickly from the basics to the 7-segment display, memory, VGA port, PS/2 port, and more - step-by-step, by example! A major revolution in digital design has taken place over the past decade. Field programmable gate arrays (FPGAs) can now contain over a million equivalent logic gates and tens of thousands of flip-flops. This means that it is not possible to use traditional methods of logic design involving the drawing of logic diagrams when the digital circuit may contain thousands of gates. The reality is that today digital systems are designed by writing software in the form of hardware description languages (HDLs). The most common HDLs used today are VHDL and Verilog. Both are in widespread use. When using these hardware description languages the designer typically describes the behavior of the logic circuit rather than writing traditional Boolean logic equations. Computer-aided design tools are used to simulate the VHDL design and to synthesize the design to actual hardware. This book assumes no previous knowledge of digital design. You start at the beginning learning about basic gates, logic equations, Boolean algebra, and Karnaugh maps. In over 75 examples we show you how to design digital circuits using VHDL, simulate them using the Aldec Active-HDL simulator, and synthesize the designs to a Xilinx Spartan3E FPGA on either the BasysTM, Nexys2TM, or Nexys3TM FPGA board. A free student edition of Active-HDL simulator is available from Aldec Inc . To synthesize your design to a Spartan3E, you will need to download the Free ISE WebPACK from Xilinx Inc. The Xilinx synthesis tools are called from within the Aldec Active-HDL integrated GUI. We will use the Adept 2 (from Digilent) utility to download your synthesized design to the Xilinx FPGA.

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