



Advanced Chip Design, Practical Examples in Verilog

Mr Kishore K Mishra

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Designing a complex ASIC/SoC is similar to learning a language well and then creating a masterpiece using experience, imagination, and creativity. Digital design starts with RTL such as Verilog or VHDL, but it is only the beginning. A complete designer needs to have a good understanding of the Verilog language, digital design techniques, system architecture, IO protocols, and hardware-software interaction that I call the **five rings of chip design**.

This book is the result of 20 years of experience and passion for chip design, love for the Verilog language, three years of focused research, and a genuine desire to share the practical design world with students and practicing engineers. I sincerely believe that you are not only going to get a jump-start, but also keep using this book for the rest of your career. **A must digital design and Verilog book** and a trusted companion that covers the five rings with plenty of real-world Verilog examples.

The book is broadly divided into two sections - chapters 1 through 10, focusing on the digital design aspects and chapters 11 through 20, focusing on the system aspects of chip design.

Chapter 3 focuses on the synthesizable Verilog constructs, with examples on reusable design (parameterized design, functions, and generate structure). Chapter 5 describes the basic concepts in digital design - logic gates, truth table, De Morgan's theorem, set-up and hold time, edge detection, and number system. Chapter 6 goes into details of digital design explaining larger building blocks such as LFSR, scrambler/descramblers, parity, CRC, Error Correction Codes (ECC), Gray encoding/decoding, priority encoders, 8b/10b encoding, data converters, and synchronization techniques.

Chapter 7 and 8 bring in advanced concepts in chip design and architecture - clocking and reset strategy, methods to increase throughput and reduce latency, flow-control mechanisms, pipeline operation, out-of-order execution, FIFO design, state machine design, arbitration, bus interfaces, linked list structure, and LRU usage and implementation.

Chapter 9 and 10 describe how to build and design ASIC/SoC. It talks about chip micro-architecture, partitioning, datapath, control logic design, and other aspects of chip design such as clock tree, reset tree, and EEPROM. It also covers good design practices, things to avoid and adopt, and best practices for high-speed design. The second part of the book is devoted to System architecture, design, and IO protocols.

Chapter 11 talks about memory, memory hierarchy, cache, interrupt, types of DMA and DMA operation. There is Verilog RTL for a typical DMA controller design that explains the scatter-gather DMA concept. Chapter 12 describes hard drive, solid-state drive, DDR operation, and other parts of a system such as BIOS, OS, drivers, and their interaction with hardware. Chapter 13 describes embedded systems and internal buses such as AHB, AXI used in embedded design. It describes the concept of transparent and non-transparent bridging.

Chapter 14 and chapter 15 bring in practical aspects of chip development - testing, DFT, scan, ATPG, and detailed flow of the chip development cycle (Synthesis, Static timing, and ECO). Chapter 16 and chapter 17 are on power saving and power management protocols. Chapter 16 has a detailed description of various power savings techniques (frequency variation, clock gating, and power well isolation).

Chapter 17 talks about Power Management protocols such as system S states, CPU C states, and device D states. Chapter 18 explains the architecture behind serial-bus technology, PCS, and PMA layer. It describes clocking architecture and advanced concepts such as elasticity FIFO, channel bonding (deskewing), link aggregation, and lane reversal. Chapter 19 and 20 are devoted to serial bus protocols (PCI Express, Serial ATA, USB, Thunderbolt, and Ethernet) and their operation.

Appendix B covers FPGA basics, and Appendix D covers SystemVerilog Assertions (SVA).

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